UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/059,427	01/29/2002	Jeroen Anton Johan Leijten	260695	6839

23460 7590 07/08/2009

LEYDIG VOIT & MAYER, LTD
TWO PRUDENTIAL PLAZA, SUITE 4900
180 NORTH STETSON AVENUE
CHICAGO, IL 60601-6731

EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
07/08/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/059,427	LEIJTEN, JEROEN ANTON JOHAN	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8 and 16-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8 and 16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/13/2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. Claims 1, 3-8, and 16-19 are pending.

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/19/2009 has been entered.

3. The office acknowledges the following papers:

Claims and arguments filed on 5/19/2009

Withdrawn Objections and Rejections

4. The drawing objection has been withdrawn due to amendment on 11/13/2006.

5. The oath objection has been withdrawn due to amendment on 11/13/2006.

Claim Objections

6. Claims 3-7 are objected to for the following reasons:

7. Claims 3-7 recite "A computer system" at line 1 that should be changed to "[[A]] The computer system" for proper antecedent basis.

8. Claim 4 recites "should be updated form" at line 2 that should be changed to "should be updated [[form]] from."

9. Claim 4 is missing a period at the end of the claim.

10. Correction is required.

New Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 1, 3-8, and 16-19 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites "the information inserted at compile time explicitly signals whether or not the subsequent memory line has to be prefetched during processing of the instruction", claim 8 recites "controlling comprises at least causing a subsequent memory line to be prefetched when the instruction is reached as a branch target", and claims 3, 17, and 19 also detail prefetching. Prefetching can be defined as loading data or instructions in anticipation of their need. However, the limitations do not actually fetch instructions in anticipation of their need, they are only fetching instructions when they are needed (i.e. when an instruction has information stating that the subsequent memory line is needed.). Therefore, what is claimed isn't prefetching as understood to one of ordinary skill in the art and is simply fetching data when it's needed. The only way that the claimed invention could possibly be considered prefetching is if the applicant is claiming a multi-cycle processor, where in the decode stage the next instruction line is fetched in anticipation of being needed a number of clock cycles in the future while the current instruction finishes executing. Since a multi-cycle processor

isn't claimed, for examination purposes, the limitation prefetching will be interpreted as simply fetching a subsequent memory line in response to the information.

13. Claim 6 recites the limitation "the functional units" in line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim. For examination purposes, no antecedent basis is established.

14. Claims 4-5, 7, 16, and 18 are rejected due to dependency.

New Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 1, 3-4, 6-8, and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (U.S. 5,819,058).

17. As per claim 1:

Miller disclosed a computer system with a processing unit and a memory, the processing unit being arranged to fetch memory lines from the memory and execute instructions from the memory lines (Miller: Figure 5 elements 26, 30-36, and 172, column 8 lines 11-29 and lines 41-62), each memory line being fetched as a whole and being capable of holding more than one instruction (Miller: Figures 7 and 8, column 8 lines 11-29 and column 11 lines 58-61)(The first line in figure 7 shows VLIW packets IP0, IP1, IP2, and IP3, which results in a single memory line containing more than a

single instruction. Column 8 states that 128 bits can be fetched at once, which is a memory line. Figure 8 shows an example of an entire memory line being fetched.), at least one instruction from the memory lines comprising information, inserted at compile time (Miller: Figure 3b element 117, column 6 lines 31-35 and lines 53-58)(Figure 3b is a compressed 32-bit instruction. The compiler performs the compression of the VLIW packets and inserts element 117 into the instructions to tell if the current instruction is at the end of a memory line or not. Element 117 reads upon information.), that signals explicitly how the processing unit, when processing the instruction from a current memory line, should control how a part of processing is affected by crossing of a boundary to a subsequent memory line (Miller: Figures 3b, 7, and 8 element 117, column 6 lines 31-35 and column 11 lines 58-67 continued to column 12 lines 1-25)(Column 6 describes a 32-bit compressed instruction containing 117 that tells if the current instruction is the last instruction within the VLIW packet. Figures 7 and 8 show examples of fetching VLIW packets from memory. IP3 and IP4 are examples of VLIW packets crossing into the subsequent memory line. Looking at figure 8, IP3 is located in memory segments 6-9 in memory lines 0 and 1. It's assumed that IP3 contains two 32-bit compressed instructions for this example. The 32-bit compressed instruction in memory segments 6-7 contains element 117 signaling not-end-of-packet since another compressed 32-bit instruction is in memory segments 8-9. Thus, element 117 will indicate that the subsequent memory line must be read out of the memory to get the whole VLIW packet to completely decompress the VLIW packet.), the processing unit being arranged to respond to the information by controlling said part of processing as

signaled by the information (Miller: Figures 7 and 8, column 11 lines 58-67 continued to column 12 lines 1-25)(IP3 and IP4 have to fetch from the next memory line due to the instruction crossing the memory boundary.), wherein information inserted at compile time explicitly signals whether or not the subsequent memory line has to be prefetched during processing of the instruction, the processing unit being arranged to start prefetching of the subsequent memory line in response to the information (Miller: Figure 3b element 117, column 6 lines 31-35 and lines 53-58)(The limitation is interpreted as fetching in view of the 112 second rejection. Miller disclosed that element 117 is inserted at compile time and indicates that the instruction is the last instruction of the memory line. It's obvious to one of ordinary skill in the art that the next instruction is then fetched from memory based on this indication.).

18. As per claim 3:

Claim 3 essentially recites the same limitations of claim 1. Therefore, claim 3 is rejected for the same reasons as claim 1.

19. As per claim 4:

Miller disclosed a computer system according to claim 1, wherein information signals explicitly whether or not an instruction pointer should be updated from a position behind the instruction in the current memory line to a start of the subsequent memory line, so that information following the instruction on the current memory line is skipped over, the processing unit being arranged to update the instruction pointer to the start of the subsequent memory line in response to the information (Miller: Figures 7 and 8, column 11 lines 35-45 and Column 12 lines 10-25)(Miller teaches that the addressing

system determines that a next instruction packet has a pad instruction in front of it. It is inherent that there is information that explicitly signals the addressing system in order for the addressing system to determine there is a pad instruction, a determination couldn't be made by hardware without an explicit signal. The pad instruction is then discarded and does not cause any operation to occur in the processor, and the Aright and Aleft addresses (program counters) are incremented to point to a new memory line, therefore the pad instruction is skipped over. The Aright address points to byte 12 in memory 282 (a subsequent memory line) and Aleft points to byte 16 (a subsequent memory line) of memory 280.)

20. As per claim 6:

Miller disclosed a computer system according to claim 1, the processing unit being a VLIW processing unit containing two or more issue slots for issuing operations from the instruction in parallel to the functional units (Miller: Figures 5, 6, and 9, column 2 lines 27-63), the instructions being VLIW instructions, capable of containing two or more operations (Miller: Figures 5, 6, and 9, column 2 lines 27-63)(The instructions are VLIW instructions that can store two or more instructions.), the instruction comprising a field distinct from the operations to specify said information (Miller: Figure 3b element 117, column 6 lines 31-35 and lines 53-58)(Element 117 is a separate field that specifies an end-of-block condition.).

21. As per claim 7:

Miller disclosed a computer system according to claim 6, the field comprising, in addition to said information, a decompression code that specifies for which issue slots

the instruction contains operations (Miller: Figures 5 and 6, column 5 lines 39-53)(The token indicates the instruction type and "identifies the processing unit.).

22. As per claim 8:

Claim 8 essentially recites the same limitations of claim 1. Claim 8 additionally recites the following limitations:

wherein said controlling comprises at least causing a subsequent memory line to be prefetched when the instruction is reached as a branch target (Miller: Figure 3b element 117, column 6 lines 31-35 and lines 53-58)(The limitation is interpreted as fetching in view of the 112 second rejection. Miller detects element 117 at decode time and fetches the next memory line. The advantage of branch instructions is that they allow for conditional execution. Official notice is given that branch instructions can execute on processors. Thus, it's obvious to one of ordinary skill in the art that the processor of Miller executes branches. Inherently, since the processor can execute branch instructions, it's possible that a taken branch can be placed as the last instruction in a memory line. Thus, the fetching occurs at the branch target.).

23. As per claims 16:

Miller disclosed the computer system of claim 1 wherein the current memory line and the subsequent memory line are positioned adjacent to the boundary (Miller: Figure 7 element IP_4)(The boundary is the crossing between lines 1 and 2. These lines are adjacent to this boundary.).

24. As per claims 17:

Miller disclosed the computer system of claim 1 wherein the prefetching of the memory line consists of prefetching a single memory line (Miller: Figure 3b element 117, column 6 lines 31-35 and lines 53-58)(The limitation is interpreted as fetching in view of the 112 second rejection. Miller disclosed that element 117 is inserted at compile time and indicates that the instruction is the last instruction of the memory line. It's obvious to one of ordinary skill in the art that the next instruction is then fetched from memory based on this indication.).

25. As per claims 18:

Claim 18 essentially recites the same limitations of claim 16. Therefore, claim 18 is rejected for the same reasons as claim 16.

26. As per claims 19:

Claim 19 essentially recites the same limitations of claim 17. Therefore, claim 19 is rejected for the same reasons as claim 17.

27. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. (U.S. 5,819,058), further in view of Keller et al. (U.S. 6,546,478).

28. As per claims 5:

Miller disclosed a computer system according to claim 1.

Miller failed to teach wherein the information signals explicitly whether or not processing of the instruction should be stalled, when the instruction is reached from a branching instruction, processing being stalled to fetch the subsequent memory line that

contains a part of the instruction, the processing unit being arranged to stall in response to the information when the instruction is reached from the branching instruction.

However, Keller disclosed information that signals (Keller: Figure 8 element 126) explicitly whether or not processing of the instruction should be stalled, when the instruction is reached from a branching instruction, processing being stalled to fetch the subsequent memory line that contains a part of the instruction, the processing unit being arranged to stall in response to the information when the instruction is reached from the branching instruction (Keller: Figure 22 element 192, column 22 lines 1-17, column 23 lines 17-24 and column 26 line 44 continued to column 27 line 8)(The detection of the continuation bit stalls processing until the next page is translated and fetched. The combination adds this bit into the branch instructions of Miller.).

This information, while associated with the instruction and addressed by the same address as the instruction, is stored in a different memory than the instruction. It would also have been obvious to combine the continuation bit 126 in the instruction itself instead of in a separate line predictor entry 82 since it has been held that the use of a one piece construction (instead of the two piece line predictor entry structure and I-cache disclosed in Keller) "would be merely a matter of obvious engineering choice." *In re Larson, 340 F.2d 965,968, 144 USPQ 347,349 (CCPA 1965).*

Adding the continuation bit to the instruction information bits that already exist would allow the processor to know whether a branch target instruction crosses a boundary in the cache and a stall should occur to fetch the next cache line. The processor could detect the need for a memory access quickly and easily if the

continuation bit was included in the cache line. The earlier a memory access is known to be needed the better, because it is well known in the art that memory accesses can be costly to processing speed. Specifically in this application, the earlier the memory access is known, the earlier the instruction is fetched from memory and the earlier the instruction can be decompressed and dispatched. It would have been obvious to combine the continuation bit within the cache line of Miller because of the advantages provided above.

Response to Arguments

29. The arguments presented by Applicant in the response, received on 5/19/2009 are partially considered persuasive.

30. Applicant argues "Presently pending claim 1 is not obvious over Miller. Miller discloses indicating to the ECU unit and processor where one compressed instruction packet ends and the next compressed instruction packet begins. *See,* Miller, column 5, lines 34-38. However, the information marking instruction packet boundaries does not indicate explicitly whether the "processing is affected by crossing of a boundary to a subsequent memory line". This depends additionally on the position of an instruction packet. Each of Miller's instruction packets will at least have an indicator that indicates the end of the packet. However this packet may be contained within a single address line (e.g. for instruction IP4, Figure 7), or at different address lines (e.g. for instruction IP3, Figure 7). Accordingly, there is no relation between the value of the end of packet indicator and the position of the instruction packet with respect to a subsequent memory

line. Let alone that the indicator can indicate "how a part of processing is affected by crossing of a boundary to a subsequent memory line." In particular the indicator does not explicitly indicate whether or not the subsequent memory line has to be prefetched during processing of the instruction. Since Miller neither discloses nor suggests each recited element of claim 1, the claim cannot be obvious over Miller alone."

This argument is not found to be persuasive for the following reason. The applicant is arguing a limitation that was upheld by the board of patent appeals and interferences. Thus, the examiner points the applicant to the rejection and to the board's decision filed on 3/19/2009 why the rejection for this limitation is maintained.

31. Applicant argues "In this regard, Mohamed discloses: "In accordance with the present invention, initially, a compiler sends to decoder unit 102 a "prefetch instruction" flag bit that indicates that a particular block of instructions, or prefetch instructions, are to be placed into prefetch instruction buffer 114, instead of instruction cache 110." *See,* Mohamed, column 3, lines 35-39. Thus, the subject-matter of amended claim 1 differs from the subject-matter disclosed by Mohamed in that the information explicitly signals whether a *subsequent memory line* should be prefetched. The "subsequent memory line" is defined in claim 1 as the *memory line subsequent to the current memory line and having a boundary therewith.* Hence Applicants' disclosed/claimed subsequent memory line is the memory line *immediately subsequent* to the current memory line."

This argument is found to be persuasive for the following reason. The examiner agrees that Mohamed failed to teach not prefetching the subsequent memory line. In response to applicant's arguments against the references individually, one cannot show

nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The combination sought to show that detecting element 117 resulted in prefetching the next memory line. However, the examiner has withdrawn the reference due to the added 112 second paragraph rejection based on the claimed prefetching. As explained above, prefetching the next memory line isn't prefetching and is simply normal fetching, especially when done with regards to detecting the information in an instruction.

32. Applicant argues "Even if the skilled person did succeed in combining the subject-matter of Miller and Keller, the resulting combination would not result in the claimed subject-matter of claim 1. In particular, the continuation field 126 of FIG. 8 of Keller referred to in the Final Office Action has a different function than the information defined in claim 1 of the present invention. The continuation field 126 merely specifies whether the line of instructions crosses *a page* boundary and does not specify whether a *boundary between current and subsequent memory lines* is crossed" for claim 5.

This argument is not found to be persuasive for the following reason. The crossing of a page boundary also means that a boundary between a current memory line and a subsequent memory line has been passed. It's just that a boundary is placed at the end of a page of data in memory. Thus, reading upon the claimed limitations.

In addition, the applicant is arguing a limitation that was upheld by the board of patent appeals and interferences. Thus, the examiner points the applicant to the

rejection and to the board's decision filed on 3/19/2009 why the rejection for this limitation is maintained.

33. Applicant argues "The token may be assigned to uncompressed instructions in any manner, however, the most compression occurs, as described above, when the shortest instruction words are assigned to the most frequently used instructions. *See,* Miller, column 5, lines 39-53. Since the token corresponds to an operations ("op") code, a control word, and a form word of an uncompressed instruction", it is definitely not distinct from the operations, as explicitly recited in Applicants' claim 6."

This argument is not found to be persuasive for the following reason. The claimed limitation states that a VLIW instruction is capable of containing two or more instructions. VLIW instructions by definition are capable of containing a plurality of operations that are stored in a long instruction word.

In addition, the applicant is arguing a limitation that was upheld by the board of patent appeals and interferences. Thus, the examiner points the applicant to the rejection and to the board's decision filed on 3/19/2009 why the rejection for this limitation is maintained.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the

objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-416262. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

/Jacob Petranek/
Examiner, AU 2183